21.5 A 92dB-DR 13mW ΔΣ Modulator for Spaceborn Fluxgate Sensors

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The read-out electronics of a state-of-the-art fluxgate magnetometer (including ADC) for scientific measurements of DC and low-frequency AC magnetic fields (<100Hz) in space and geophysics, which requires a >1,000nT measurement range and a SNR of more than 90dB, is normally placed on a large PCB (100cm^2) and consumes more than 350mW. It is essential for future space applications, especially onboard miniaturized satellites and landing units, that the size and power of the read-out circuit be reduced while keeping a suitable SNR and radiation hardness.

Figure 21.5.1 shows how the traditional control loop of a fluxgate magnetometer can be combined with the control loop of a 2nd-order ΔΣ modulator [1]. A fluxgate sensor is usually made with a soft-magnetic core (ring or rod) placed in the center of a solenoid pick-up coil. The core is wrapped with a single layer of drive windings, which are then periodically driven by current pulses with a frequency f_0 of 5 to 20kHz in order to periodically saturate the magnetic material. The output signal from the pick-up coil then contains induced even harmonics of f_0 that are proportional to the external magnetic field [2]. The readout electronics extracts the magnetic field information by synchronously converting and integrating the 2nd-harmonic term ($2f_0$). Normally, the fluxgate sensor operates as a zero detector since the output voltage is fed back via a resistor to either the pick-up coil or a separate feedback coil in order to increase the overall linearity. When combining the fluxgate control loop with a 2nd-order ΔΣM, the input junction point can be placed directly in the fluxgate sensor and the integrator, which helps to demodulate the field information, can be merged with the first integrator of the ΔΣM.

The ASIC design presented here is based on a 2-2 cascaded ΔΣM [3], whereas the first of the two 2nd-order modulators is adapted as explained in Fig. 21.5.1. The type of ΔΣM was chosen to overcome the stability problems of higher-order single-loop modulators, to ensure high linearity, and to provide a simple feedback connection to the external fluxgate sensor (because of its 1b quantization). It is operated at $f_0/2$ = 8.192kHz.

The linearized model of the implementation is depicted in Fig. 21.5.2. It consists of the modified 2nd-order ΔΣM (fluxgate sensor, input amplifier, synchronous demodulator, two integrators and quantizer) and an unmodified 2nd-order ΔΣM. The outputs of the modulators are further connected to an error cancellation logic circuit, which combines the two 1b inputs into a 6b output with a 4th-order noise shaping characteristic. The sensor is modelled by its feedback factor S_{FB} (in nT/μA), which describes the feedback coil, and by its sensitivity S_{SE} (in μV_{eff}/nT @ $2f_0$), which represents the pick-up coil and the summing node. The input amplifier is operated as a band-pass filter with a gain of G_{IA} at $2f_0$. The phase adjustable synchronous demodulator (ASD) of the model is a simple gain stage with G_{SD} equal to $\sqrt{2}\cdot 2/\pi$ (inverted form factor). The feedback resistor R_{FB} sets the current through the feedback coil and thus determines the measurement range.

The combined ASD and first integrator (I1) stage runs at $2f_0$ and is realized by a SC integrator with additional input switches (see Fig. 21.5.3). The ASD clock (CMOD and CMODX) can be shifted by digital commands to maximize the rectified output signal. Integrator 1 runs at a higher clock rate ($f_I = 16f_0$, CP1 and CP2) in order to properly integrate the rectified ASD output.

This higher clock rate shifts the I1 gain from

$$G''_{11} = \frac{C_S}{C_I} \quad \text{to} \quad G'_{11} = \frac{f_I}{f_0/2} G''_{11} = 32\, G''_{11}.$$

To ensure 4th-order noise shaping and good pattern noise rejection the gain factors of the 1st and 2nd stages must be matched:

$$G_{11} = \frac{1}{R_{FB}} S_{FB} S_{SE} G_{IA}\, 2\, \frac{\sqrt{2}}{\pi} G'_{11} = G_{21} = 0.5.$$

The gains G_{IA} and G'_{11}, as well as the feedback resistor R_{FB}, are adjustable in order to keep the ASIC usable for different fluxgate sensors. R_{FB} and G_{IA} are set by external components and G'_{11} by switches in the capacitor network in Fig. 21.5.3, which can be activated by a digital command.

The chip contains 3 modified 2-2 cascaded modulators (fluxgate channels) for a 3D measurement of the magnetic field plus an additional conventional 2-2 cascaded modulator (voltage channel) with an 8:1 multiplexer for auxiliary measurements. The digital part contains a 4th-order sinc-filter for each channel (OSR = 64) with an output data rate of 128Hz. In addition, the data rate can be further lowered by factors of 2 down to 2Hz by using boxcar filters. The command and telemetry interface is realized with a serial synchronous interface.

The PSD plots of the voltage (range: ±1.25V) and fluxgate channels (range: ±2,000nT) are depicted in Fig. 21.5.4. Both the voltage and fluxgate channels (with G_{11}=0.5) show 4th-order noise shaping, but the noise floor of the fluxgate channel below 100Hz is 6dB higher due to the noise from the fluxgate sensor and the input stage of the modified ΔΣM. The noise densities of both channels increase at lower frequencies because of the flicker noise in the first integrator. The 4th-order performance of the fluxgate channel decreases significantly when the G_{11}-factor is off by about 10%. The SNDR of the voltage channel, which was calculated with the output data of the sinc-filter (-3dB at 30Hz) and an input sine at 10Hz, is shown in Fig. 21.5.5. The SNDR and DR are 92dB and 98dB, respectively. The DR of the decimated output of the fluxgate channel in a bandwidth of 0.1 to 30Hz measured 92dB for field ranges of more than ±2,000nT. For lower ranges, the DR decreases because of the range-independent sensor noise.

The chip was also tested for its radiation sensitivity to total ionizing dose (TID, [4]) up to 260krad, and its susceptibility to single event latch-ups (SEL, [5]) caused by heavy ions. All tested chips showed full functionality throughout the complete TID test run as well as after irradiation. The SNDR decreased by 0.04dB·krad^{-1} and the digital supply current increased slightly by 6μA·krad^{-1}. The SEL test showed that the chip latches at a linear energy transfer (LET) of 14.1MeV·cm^2·mg^{-1}.

The chip was fabricated in a 0.35μm 2P4M CMOS technology and a micrograph is shown in Fig. 21.5.6. The overall power dissipation of all four channels is 49mW (13mW per fluxgate channel and 10mW for the voltage channel) at a supply voltage of 3.3V. The area is 20mm^2 and the die is located in a CQFP-100 package.

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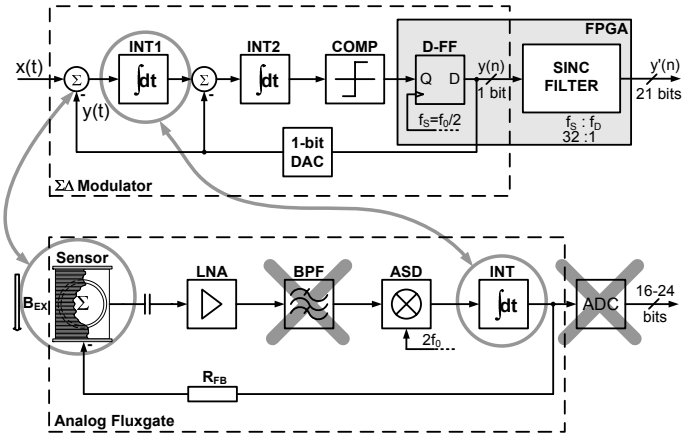

Figure 21.5.1: Merging a 2nd-order ΔΣ modulator with a fluxgate control loop.

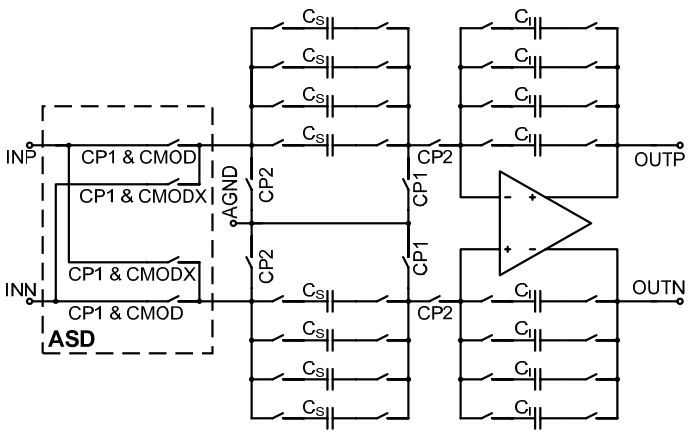

Figure 21.5.3: SC integrator with ASD and variable gain setting.

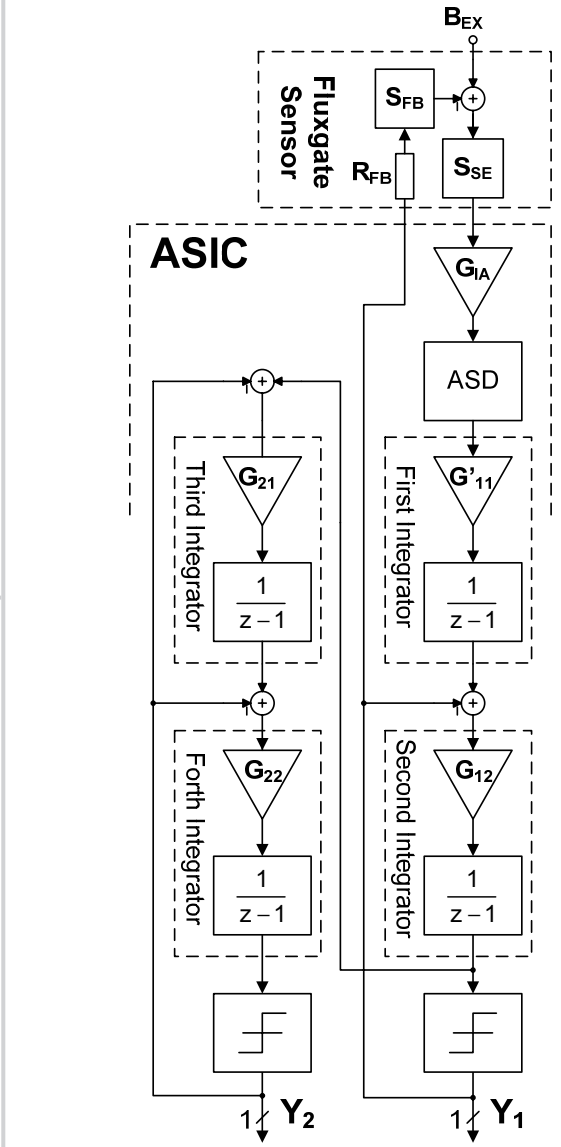

Figure 21.5.2: Linearized model of the modified 2-2 cascaded ΔΣM.

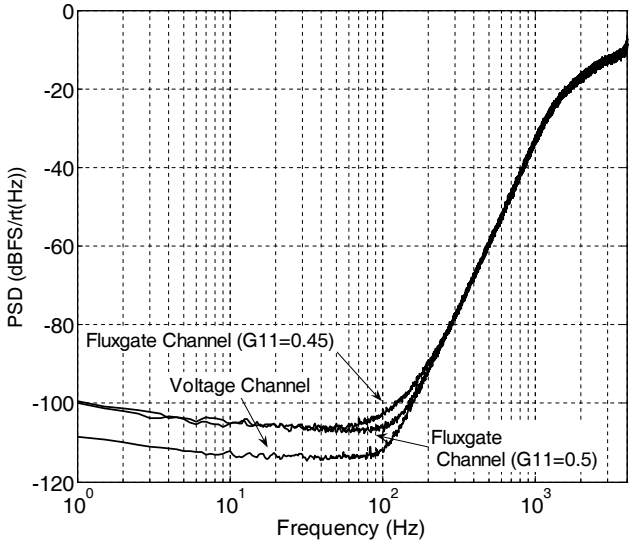

Figure 21.5.4: PSDs of fluxgate and voltage channels.

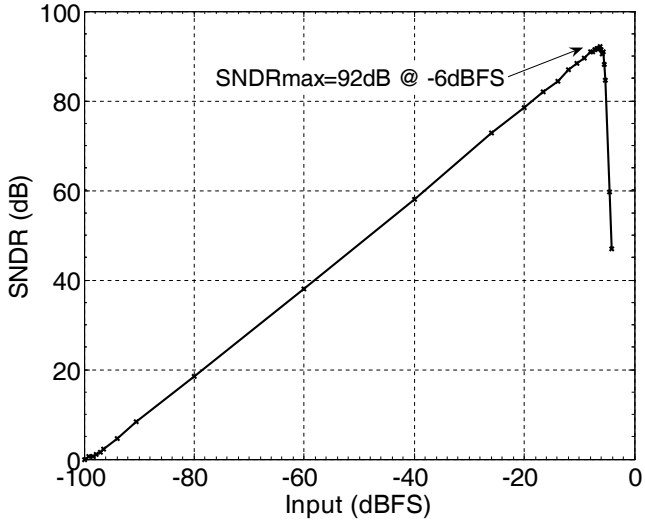

Figure 21.5.5: SNDR of the voltage channel.

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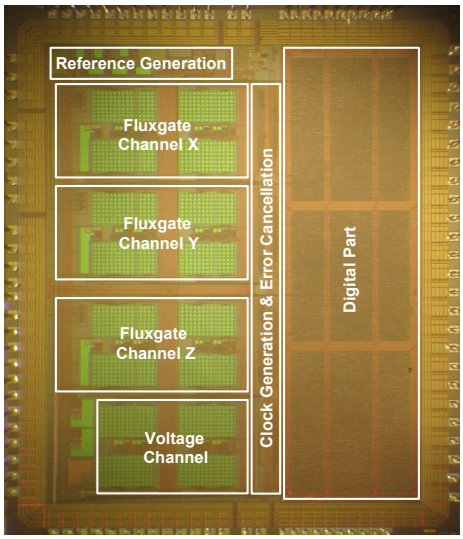

Figure 21.5.6: Chip micrograph.

